Bell Laboratories in USA were the first to fabricate a silicon based semiconductor device called thyristor. Its first prototype was introduced by GEC (USA) in 1957. This company did a great deal of pioneering work about the utility of thyristors in industrial applications. Later, many other devices having characteristics similar to that of a thyristor were developed. These semiconductor devices, with characteristics identical with that of a thyristor, are TRIAC, DICR, SCS, SUS, PUT, LASCR etc. This whole family of semiconductor device is given the name thyristor. Thus, the term thyristor denotes a family of semiconductor devices used for power control in dc and ac system.

One oldest member of this thyristor family called silicon-controlled rectifier (SCR) is the most widely used device. At present, the use of SCR is so vast that over the years, the word thyristor has become synonymous with SCR.

The name 'thyristor' is derived by a combination of the capital letters from THYRation & TRANSITOR. This means that thyristor is a solid state device like a transistor & has characteristics similar to that of a thyatron tube.
Thyistor family symbols & characteristics:

1. **SCR**
   - $V_{\text{max}} = 7000 \, \text{V}$
   - $I_{\text{max}} = 5000 \, \text{A}$

2. **TRIAC**
   - $P.J. \, \text{Shah}$
   - ($1200 \, \text{V}, 1000 \, \text{A}$)

3. **DIAC**

4. **SCS** (Silicon Controlled Switch)
   - ($100 \, \text{V}, 200 \, \text{mA}$)
5) **SUS** (Silicon Unilateral Switch)

6) **LASCR**

7) **PUT**
1) BJT

2) MOSFET

3) GTO (Gate Turn off Thyristor)

4) IGBT (Insulated Gate Bipolar Transistors)

5) MCT (MOS-Controlled Thyristor)

6) FCT (Field-Controlled Thyristor)
THYRISTORS FAMILY

SCR (Silicon-Controlled Rectifier)

SCR is the most widely-used member of the family of the thyristors. The SCR is a four-layer device with three terminals, namely, the anode, the cathode & the gate.

When anode is made positive with respect to the cathode, junction J2 is reverse-biased & only the leakage current will flow through the device. The SCR is then said to be in the forward blocking state or off-state.

When the cathode is made positive with respect to the anode, junction J1 & J3 are reverse-biased and a small reverse leakage current will flow through the SCR. This is the reverse blocking state of the device.

When the anode-to-cathode voltage is increased, the reverse-biased junction J2 will break down due to the large voltage gradient across the depletion layers. This is the avalanche breakdown.

Since the other junctions J1 & J3 are forward-biased, there will be free carrier movement across all three junctions, resulting in a large anode-to-cathode forward current IT. The voltage
drop $V_T$ across the device will be the \textit{on} state. The drop in the four layers of the device, if they are said to be in the conducting state or \textit{on}-state.

\textbf{SCR Characteristics:}

![Diagram showing SCR characteristics]

Fig. 1 shows the characteristics of an SCR. In the \textit{on}-state, the current is limited by the external impedance. If the anode-to-cathode voltage is now reduced, since the original depletion layer and the reverse-biased junction $J_2$ no longer exist due to the free movement of carriers, the device will continue to stay on.

When the forward current falls below the level of the holding current $I_h$, the depletion region will begin to develop around $J_2$ due to the reduced no. of carriers of the device, and the device will go to the \textit{blocking} state.

Similarly, when the SCR is switched on, the resulting forward current has to be more than the holding current $I_h$. This is necessary for maintaining the required amount of carriers flow across the junction; otherwise, the device will return to the \textit{blocking} state as soon as the anode-to-cathode voltage is reduced.
The holding current is usually lower than, but very close to, the latching current; its magnitude is of the order of a few milliamperes (mA).

When the SCR is reverse-biased, the device will behave in the same manner as two diodes connected in series with reverse voltage applied across them. The thinner two regions of the SCR will be lightly doped as compared to the outer layers. Hence, the thickness of the \( J_2 \) depletion layer during the forward-bias conditions will be greater than the total thickness of the two depletion layers at \( J_1 \) and \( J_3 \) when the device is reverse-biased. Therefore, the forward breakdown voltage \( V_{BO} \) will be greatly higher than the reverse breakdown voltage \( V_{BR} \). The forward current of the device at the breakdown point is denoted by \( I_0 \).

SCR has two stable & reversible operating states. The changeover from off-state to on-state, called turn-on, is achieved by increasing the forward voltage beyond \( V_{BO} \). The reverse transition, termed turn-off, is made by reducing the forward current below \( I_0 \). A more convenient and useful method of turning on the device employs the gate drive. If forward voltage less than \( V_{BO} \) is applied across the device, it can be turned on by applying a positive voltage between gate & the cathode. This method is known as gate control.
Fig. shows the two-transistor model of an SCR. This is obtained by splitting the two middle layers into two separate parts. The collector current of transistors T1 becomes the base current for T2, of vice versa. If \( \alpha_{b1} \) and \( \alpha_{b2} \) are the common base current gains for T1 and T2 respectively, it can be easily derived from Fig. that with a forward voltage applied across the anode and the cathode, if the gate terminal left free, the forward blocking current is

\[
I_D = I_C \left( 1 - \frac{\alpha_{b1} + \alpha_{b2}}{\alpha_{b1}} \right) \quad (1)
\]

where \( I_C \) is the reverse leakage current of the reverse-biased junction \( J_2 \) when the two outer layers are not present. In silicon transistors, \( \alpha_{b} \)s are dependent on the emitter current.

Therefore, initially when the applied forward voltage is small \((\alpha_{b1} + \alpha_{b2}) < 1\), \( I_D \) will be less than \( I_C \), and at some level \((\alpha_{b1} + \alpha_{b2}) = 1\), it will become equal to \( I_C \). Under these conditions, the value of \( I_D \) will be equal to \( I_C \). The internal regeneration will begin if the device will go to the on-state. This can be seen from eq. (1) above.
When \((X_b + X_{b2})\) approaches unity, current \(I_D\) will tend to infinity.

The transistor analogy of eqn 1 are not valid when the device goes into conduction. The forward current is then limited by the external impedance and not by the base current of the turn transistor model.

The device can go back to the off-state only when the forward current falls below \(I_{th}\), at which instant the \(X_b\) will be very low, \((X_b + X_{b2})\) will be less than 1, and internal regeneration will stop.

The reverse leakage current \(I_{co}\) can be increased by raising the applied forward voltage. When this voltage is equal to \(V_{th}\), the value of \((X_b + X_{b2})\) will become 1, and the device will go to the on-state. A rise in the junction temp. will increase \(I_{co}\) and cause breakdown.

Silicon is used as the intrinsic semiconductor in the fabrication of an SCR to improve its thermal stability and to keep the value of \(X_b\) small at normal junction temperature. With gate current \(I_g\) flowing into the base of transistor \(T_2\), eqn 1 becomes,

\[
I_D = \frac{(I_g + I_{co})}{1 - (X_b + X_{b2})}
\]

Thus, the effect of applying a positive voltage between the gate and the cathode, when the device is forward biased, is that the leakage current through junction \(T_2\) is increased. This is because the resulting gate current consists mainly of electron flow from the cathode to the gate (since the bottom N layer is heavily doped as compared to the gate P layer). Due to the applied voltage gradient, some of these electrons reach region \(T_2\) and add to the minority carrier concentration in the P layer near junction \(T_2\). This raises the reverse leakage current and consequently lead to a breakdown.
even though the applied forward voltage is lower than $V_{ao}$ and the junction temp. is normal. Thus, the gate provides a very convenient method for switching the device from off-state to on-state, with low anode-to-cathode voltages. When the device is turned on, all four layers will be filled with carriers, and even if the gate supply is removed, the device will continue to stay on due to internal regeneration. Therefore, a gate signal is required only for turning on the SCR. For low- to medium-power SCRs, the gate current also is in the mA range.

Derivation for

$$I_A = \frac{\alpha_2 \cdot I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

The collector current of a thyristor is related in general to the emitter current $I_E$ and the leakage current of the collector-base junction $I_{CBO}$ as:

$$I_C = \alpha \cdot I_E + I_{CBO}$$  \(\text{(1)}\)

Common-base current gain is defined as

$$\alpha \equiv \frac{I_C}{I_E}$$
For transistor Q1, the emitter current is the anode current $I_A$ and the collector current $I_{C1}$ can be found from eqn 1

$$I_{C1} = \alpha_1 I_A + I_{CBO1}$$

where $\alpha_1$ is the current gain for $Q1$, $I_{CBO1}$ is the leakage current for $Q1$.

Similarly, for $Q2$, the collector current $I_{C2}$ is

$$I_{C2} = \alpha_2 I_k + I_{CBO2}$$

where $\alpha_2$ is the current gain for $Q2$, $I_{CBO2}$ is the leakage current for $Q2$.

By combining $I_{C1}$ & $I_{C2}$, we get

$$I_A = I_{C1} + I_{C2} \Rightarrow$$

$$= \alpha_1 I_A + I_{CBO1} + \alpha_2 I_k + I_{CBO2}$$

But for a gating current $I_g$:

$$I_k = I_A + I_g$$

Solving eqn 2 for $I_A$ given

$$(4) \Rightarrow I_A = \alpha_1 I_A + \alpha_2 (I_A + I_g) + I_{CBO1} + I_{CBO2}$$

$$I_A - \alpha_2 I_A = \alpha_1 I_A + \alpha_2 I_g + I_{CBO1} + I_{CBO2}$$

$$I_A = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_2 + \alpha_1)}$$

The current gain $\alpha_1$ varies with the emitter current $I_A = I_E$; and $\alpha_2$ varies with $I_k = I_A + I_g$. A typical variation of current gain $\alpha$ with the emitter current $I_E$ is shown in Fig.2.
Methods of Turning ON

SCR can be switched into conduction either by increasing the forward voltage beyond V_{th} or by applying a positive gate signal when the device is forward biased.

Of these two methods, the latter, called the gate-control method, is used as it is more efficient and easy to implement for power control.

The following points have to be noted when designing the gate-control circuit:
1. Appropriate gate-to-cathode voltage must be applied for turn-on when the device is forward biased.
2. The gate signal must be removed after the device is turned on.
3. No gate signal should be applied when the device is reverse biased.
4. When the device is in off-state, a negative voltage applied between the gate and the cathode will improve the characteristics of the device. In such an instance, a large positive voltage will be required to overcome this negative bias for turn-on.

There are three ways of triggering the device by gate control:

Triggering by an AC Gate Signal

In many power-control circuits that use AC input, the gate-to-cathode voltage is obtained from a phase-shifted AC voltage derived from the main supply. The advantage of this scheme is that proper isolation of power-control circuit can be provided.

The firing angle control is obtained very conveniently by changing the phase angle of the control signal. However, gate drive is maintained for one half-cycle after the device is turn-on.
and a reverse voltage is applied between the gate and the cathode during the negative half-cycle.

Triggering by a DC Gate Signal:

A DC voltage of proper polarity and magnitude is applied between the gate and the cathode when the device is to be turned on. It must, however, be remembered that the SCR is a current-operated device and it is the gate current (injected carriers) that turns on the device.

The drawbacks of this scheme are that the gate-signal has to be continuously applied (resulting in an increase in internal power dissipation) and that there is no isolation of the gate-control circuit from the main power circuit.

Triggering by a pulsed-Gate Signal:

The gate drive consists of a single pulse appearing periodically, or a sequence of high-frequency pulses. This is known as carrier frequency gating. A pulse transformer is used for isolation. The gate losses are very much reduced since the drive is discontinuous.

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Methods of turning on a thyristor with forward voltage

- Forward voltage triggering
- dV/dt triggering
- Temperature triggering
- Light triggering

2. Forward Voltage Triggering

When anode to cathode forward voltage is increased with gate circuit open, the reverse biased junction J₂ will have an avalanche breakdown at a voltage called forward breakdown voltage (V₉₀). At this voltage, thyristor changes from OFF-state to ON-state characterised by low voltage across thyristor with large forward current. The forward current is limited mainly by the load impedance. The forward voltage drop across SCR during the ON-state is of the order of 1 to 1.5 V and increase slightly with load current.

3. dV/dt Triggering

With forward voltage across the anode and cathode of a thyristor, the two outer junction are forward biased but the inner junction is reverse biased. This reverse bias junction J₂ has the characteristic of a capacitor due to charge existing across the junction. If the entire anode to cathode forward voltage Vₐ appears across J₂, the charge is denoted by Q, then charging current is given by:

\[ i = \frac{dQ}{dt} = \frac{1}{C_j} \frac{d(V_a)}{dt} = C_j \frac{dV_a}{dt} + V_a \frac{dC_j}{dt} \]

As C_j, the capacitance of junction J₂, is almost constant, the current is given by

\[ i = C_j \frac{dV_a}{dt} \]
If the rate of rise of forward voltage \(dv/dt\) is high, the charging current \(I\) will be more. This charging current plays the role of gate current and turns on the SCR even when gate signal is gone. Such phenomena of turning on a thyristor, called \(dv/dt\) turn-on, must be avoided as it lead to false operation of the thyristor circuit.

For controllable operation of the thyristor, the rate of rise of forward anode to cathode voltage \(dv/dt\) must be kept below the specified rated limit. Typical values of \(dv/dt\) are 20-500 V/sec. False turn-on of a thyristor by large \(dv/dt\) can be prevented by using a snubber circuit in parallel with the device.

C) Temperature Triggering:

During forward blocking, most of the applied voltage across reverse biased junction \(J_2\). This voltage across junction \(J_2\) associated with leakage current may raise the temperature of this junction. With increase in temp., leakage current through junction \(J_2\) further increases. This cumulative process may turn on the SCR at some high temp.

D) Light Triggering:

When light is thrown on the gate-cathode junction \(J_3\) through a light window, free charge carriers (holes & electrons) are generated. If the intensity of this light exceeds a certain value, the SCR is turned on. Such a thyristor is known as light-activated SCR (LASCR)
Dynamic Characteristics of SCR

During the turn-on and turn-off processes, a thyristor is subjected to different voltages across it at different currents through it. The time variation of the 0 voltage across a thyristor and the current through it during turn-on and turn-off processes give the dynamic or transient characteristics of a thyristor.

Turn-on Characteristics

- A forward biased thyristor is usually turned on by applying a positive gate voltage between gate and cathode. This results in a transition time from forward off-state to forward on-state.
- This transition time, called thyristor turn-on time, is the sum of the delay time $t_{dl}$ and the rise time $t_r$. It can be observed that the total turn-on time depends on the anode circuit parameters, the gate signal amplitude $I_{g}$, and the rise time $t_r$. The turn-on time is of the order of 2-4 usec.

Delay time $t_{dl}$ - The delay time $t_{dl}$ is measured from the instant at which gate current reaches 0.1 $I_{g}$ to the instant at which anode current
reaches 0.1 \( I_T \).

The delay time may also be defined as the duration between the instant gate current reaches 0.1 \( I_T \) to the instant anode voltage falls to 0.9 of its initial value.

Rise time \( t_r \): The rise time \( t_r \) is the time taken by the anode current to rise from 0.1 \( I_T \) to 0.9 \( I_T \). The rise time is also defined as the time required for the forward blocking off-state voltage to fall from 0.9 to 0.1 of its initial value. The rise time value is inversely proportional to the magnitude of gate current and its build-up rate.

**Turn-off characteristics**

![Graph showing turn-off characteristics of an SCR](image)

When an SCR is turned on by the gate signal, the gate loses control and device can be brought back to the blocking state only by reducing the forward current to a level below that of the holding current. In RC circuits where the current goes through a natural zero value, the device will be automatically turned off. In such circuit, the SCR has to be triggered synchronously with the zero crossing of the input voltage in every positive half-cycle.
In the applied AC voltage, in DC circuits where there is no natural zero value of the current, the forward current can be reduced either by shunting the SCR by another device or by applying a reverse voltage across the anode and the cathode of the SCR through the SCR to zero.

In any circuit in reverse voltage applied, this reverse voltage will sweep out the excess carriers (electrons from the bottom N layer and holes from the top P layer) from the two outer layers, and thus facilitate the turn-off. In this process a reverse recovery current will be set up. It is evident that this negative current can be much greater than the conventional reverse blocking current $I_{BR}$ of the device. The excess carriers in the inner two regions can decay only due to recombination. Thus, the total turn-off time $t_q$ required for the device is the sum of the duration for which the reverse recovery current flows after the application of reverse voltage ($t_{rr}$) and the time required for the recombination of all excess carriers in the inner two layers of the device ($t_{br}$).

At the end of this turn-off time, a depletion layer develops across junction $J_2$ and the device can then withstand the forward voltage. The turn-off time is dependent on the anode current $I_A$, the magnitude of the reverse voltage applied, and the magnitude of the rate of application of the forward voltage.

The turn-off time $t_q$ normal cases is of the order of 50-100 μsec, and for high frequency cases it is about 10-20 μsec.
The reliable operation of an SCR, like that of any other semiconductor device, can only be ensured when its ratings are not exceeded during the on- or off-state. The specifications of the device relate to its current-carrying capacity and voltage withstanding capability. The junction temp. has a direct bearing on the performance of the device since it affects the carrier densities in the four layers. It is for this reason that the forward and reverse break-over voltages will be lower as the temp. increases. Similarly, the turn-off time will increase with temp. for a given forward current, and the minimum gate current required for turn-on will be lower.

The junction temp. will be a function of the internal losses of the device and the efficiency of the heat transfer mechanism.

The following factors contribute to internal losses:

i) The on-state forward voltage drop across the device (V_T).

ii) The off-state forward and reverse current (I_D, I_D_R).

iii) The gate current (I_G).

The off-state losses include both forward and reverse blocking conditions. The gate losses can be reduced by pulse-firing. A properly designed heat sink will reduce the temp. rise of the junction.
The most convenient method of switching on a forward-biased SCR is by applying a positive voltage between the gate and the cathode. As far as its internal mechanism for turning on is concerned, the process is the same as that of applying a gate drive to a conventional SCR which increases the minority carrier density in the inner P layer thereby facilitating the reverse breakdown of junction J2. It may also be mentioned that there are maximum and minimum limits for gate voltage and gate current to prevent permanent destruction of junction J2 and to provide reliable firing.

Similarly, there is a limit on the maximum instantaneous gate power dissipation ($P_{max} = V_g I_g$). The permissible maximum value of $P_{max}$ depends on the type of gate drive.

The gate signal can be DC or AC (normally at power frequency), or a sequence of high-frequency pulses. With pulse-firing, a larger amount of instantaneous gate power dissipation can be tolerated if the average...
Value of I_g is within the permissible limits. In other words, the gate can be driven harder (greater V_g and I_g) when pulse-firing is used. This provides for reliable and faster turn-on of the device.
Gate Triggering Circuit 8.

Gate triggering is the most common method of turning on SCRs, because this method tends itself accurately for turning on the SCR at the desired instant of time. Gate triggering is an efficient and reliable method.

A firing circuit should fulfill the following two functions. (Main features).

1) If the circuit has more than one SCR, the firing circuit should produce gating pulses for each SCR at the desired instant for proper operation of the power circuit. These pulses must be periodic in nature and the sequence of firing must correspond with the type of thyristor power controller.

2) The control signal generated by a firing circuit may not be able to turn-on an SCR directly. It is therefore common to feed the voltage pulses to a driver circuit and then to gate-cathode circuit. A driver circuit consists of a pulse amplifier and a pulse transformer.

![Diagram](image)

Fig. A general layout of the firing circuit scheme for SCRs.

A firing scheme, in general, consists of the components. A regulated dc power supply is obtained from an alternating voltage source. Pulse generator, supplied from both ac and dc sources, gives out voltage pulses which are then fed to pulse amplifier for their amplification. Shielded cables transmit the amplified pulses to pulse transformers. The
The function of the transformer is to isolate the low-voltage gate-cathode circuit from the high-voltage anode-cathode circuit. Some firing circuit schemes are:

1) Resistance firing circuit,
2) Resistance-capacitance firing circuit,
3) UJT firing circuit.

R and RC firing circuits are not in commercial use these days. They offer simple and economical firing circuits.

### R-Firing Circuit

Resistance triggering circuits are the simplest and most economical. They have limited range of firing angle control (0° to 90°), great dependence on temperature and differences in performance between individual SCR's.

![Resistance Firing Circuit Diagram](image)

Fig. shows the most basic resistance triggering circuit. $R_2$ is the variable resistance, $R$ is the stabilizing resistance.

In case $R_2$ is zero, gate current may flow from source, through load, $R_1$, D and gate to cathode. This current should not exceed maximum permissible gate current $I_{gm}$. $R_1$ can therefore be found from the relation:

$$\frac{V_m}{R_1} \leq I_{gm} \text{ or } R_1 \geq \frac{V_m}{I_{gm}}$$

where $V_m$ is maximum value of source voltage.

The function of $R_1$ is to limit the gate current to a safe value as $R_2$ is varied.

Resistance $R$ should have such a value that maximum voltage drop across it does not exceed maximum possible gate voltage $V_{gm}$. 
This can be happen only when \( R_2 \) is zero.

Under this condition,

\[
\frac{V_m}{R + R_b} \leq V_{gm} \quad \text{(voltage divider)}
\]

or

\[
\frac{V_m \cdot R}{R + R_b} \leq V_{gm} \cdot (R_1 + R)
\]

\[
V_m \cdot R \leq V_{gm} \cdot R_1 + V_{gm} \cdot R
\]

\[
R \left( V_m - V_{gm} \right) \leq V_{gm} \cdot R_1
\]

\[
R \leq \frac{V_{gm} \cdot R_1}{V_m - V_{gm}}
\]

As resistance \( R_1, R_2 \) are large, gate trigger circuit draws a small current. Diode \( D_1 \) allows the flow of current during positive half cycle only, i.e., gate voltage \( V_g \) is half-wave rectifier pulse. The amplitude of this rectifier pulse can be controlled by varying \( R_2 \).

The potentiometer setting \( R_2 \) determines the gate voltage amplitude. When \( R_2 \) is large, current \( i \) is small and the voltage across \( R_1 \) is \( V_g = iR_1 \) is also small as shown in (i) and (ii).
As \( V_{gp} \) is less than \( V_{gt} \), SCR will not turn on. Therefore, load voltage \( V_o = 0 \), \( i_o = 0 \) and supply voltage \( V_g \) appears as \( V_f \) across SCR, as shown in Fig 9 @.

In Fig 9 b, \( R_2 \) adjusted such that \( V_{gp} = V_{gt} \). This gives the value of firing angle as 90°. The various current and voltage waveform are shown in Fig 9 c.

In Fig 9 c, \( V_{gp} > V_{gt} \), as soon as \( V_g \) becomes equal to \( V_{gt} \) for the first time, SCR is turned on. The resistance triggering cannot give firing angle beyond 90°. Increasing \( V_g \) above \( V_{gt} \) causes on the SCR at firing angles less than 90°.

A relationship between peak gate voltage \( V_{gp} \) and gate trigger voltage \( V_{gt} \) can be expressed as follows:

\[
V_{gp} \sin \alpha = V_{gt}
\]

\[
\alpha = \sin^{-1} \left( \frac{V_{gt}}{V_{gp}} \right)
\]

Since \( V_{gp} = \frac{V_{m}R}{R_1 + R_2 + R} \)

\[
\alpha = \sin^{-1} \left[ \frac{V_{gt} \cdot (R_1 + R_2 + R)}{V_{m}R} \right]
\]

As \( V_{gt}, R_1, R_2 \) and \( V_{m} \) are fixed, \( \alpha \propto \frac{1}{R_2} \)

This is shows that firing angle \( \alpha \) is proportional to \( R_2 \). As \( R_2 \) is increased from small value, firing angle increases. In any case, \( \alpha \) can never be more than 90°.

As the firing angle is from 0° (approx) to 90°, the half wave power output can be controlled from 100% (for \( \alpha = 0° \)) down to 50% (for \( \alpha = 90° \)).
RC Firing Circuit

The limited range of firing angle control by R firing circuit can be overcome by RC firing circuit.

The circuit diagram shows the RC half-wave trigger circuit. By varying the value of R, firing angle can be controlled from 0° to 180°. In the negative half cycle, capacitor C charges through D2 with lower plate positive to the peak supply voltage Vm. This capacitor voltage remains constant at -Vm until supply voltage attains zero value. Now as the SCR anode voltage passes through zero and becomes positive, C begins to charge through variable R from the initial voltage -Vm. When capacitor charges to positive voltage equal to gate trigger voltage Vgt, SCR is fired and after this capacitor holds to a small positive voltage.
Diode D1 is used to prevent the breakdown of cathode to gate junction through D2 during the negative half cycle.

In the range of power frequencies, \( V_0 \) may be empirically shown that \( R \) for zero output voltage is given by,

\[
RC \geq \frac{1.5}{f} \approx \frac{4}{\omega}
\]

\( T = \frac{1}{f} \) = period \( f \) ac line frequency in sec.

The SCR will trigger when \( V_e = V_{gt} + V_d \)

where \( V_d \) is the voltage drop across diode D1.

At the instant of triggering, if \( V_e \) is assumed constant, the current \( I_{gt} \) must be supplied by voltage source through \( R \), D1, and gate to cathode circuit. Hence, the maximum value of \( R \) is given by

\[
V_e \geq R \cdot I_{gt} + V_d
\]

or

\[
V_e \geq R \cdot I_{gt} + V_{gt} + V_d
\]

or

\[
\frac{V_e + V_d}{R} \geq I_{gt}
\]

where \( V_e \) is the source voltage at which thyristor turns on.

When SCR triggers, voltage drop across it falls to 1 to 1.5 V. This, in turn, lowers the voltage across \( R \) and \( C \) to this low value of 1 to 1.5 V. Low voltage across SCR during conduction period keeps C discharged in positive half cycle until negative voltage cycle across C appears. This charges C to max. negative - \( V_m \) as shown in fig by dotted line. In fig \( R \) is more and therefore average output voltage is low. In fig \( R \) is less, firing angle is low and therefore average output voltage is more.
UJT Triggering Circuit

The UJT is commonly used for generating triggering signals for SCRs. The basic UJT relaxation oscillator is used for this generating trigger pulses.

Synchronized UJT Triggering (or Ramp Triggering)

Fig. shows a synchronized UJT trigger circuit using an UJT, diodes (D1-D4) rectified as to AC. Resistor R₁ lowers Vdc to a suitable value for the zener diode and UJT. Zener diode Z functions to clip the rectified voltage to a standard level V₈, which remains constant except near the Vdc zero, as Fig. a.

This voltage V₈ is applied to the charge circuit RC. Current i₁ charges capacitor C at a rate determined by R. Voltage across capacitor is marked by Vc in Figs. When voltage Vc reaches the unijunction threshold
voltage $V_{BZ}$, the EBJ junction of UJT breakdown and the capacitor $C$ discharges through primary of pulse transformer sending a current $i_2$ as shown in Fig. 7. As the current in is in the form of pulse, windings of the pulse transformer have pulse-voltage at their secondary terminals. Pulses at the two sec. windings feed the same envelope pulse to the SCR of a full-wave circuit. SCR with positive anode voltage would turn on. As soon as the capacitor discharges, it starts to recharge as shown. Rate of rise of capacitor voltage can be controlled by varying $R$. The firing angle can be controlled up to about 150°. This method of controlling the output power by varying charging resistor $R$ is called ramp control, open-loop control or manual control.

As the average voltage $V_{BZ}$ goes to zero at the end of each half cycle, the synchronization of the trigger circuit with the supply voltage across SCR is achieved.
Ramp and pedestal triggering is an improved version of synchronized UJT oscillator triggering. In Fig two SCR's connected in antiparallel for controlling power in an AC load. This trigger circuit can also be used for triggering the thyristors in single-phase semi-converter or full converter.
Zener diode voltage \( V_2 \) is constant at 1.5V.

Threshold voltage \( R_2 \) acts as a potential divider.

Wiper of \( R_2 \) controls the value of pedestal voltage \( V_{pd} \). Diode \( D \) allows \( C \) to be quickly charged to \( V_{pd} \) through the low resistance of the upper portion of \( R_2 \).

The setting of wiper on \( R_2 \) is such that this value of \( V_{pd} \) is always less than the Zener firing point voltage \( ZV_2 \). When wiper setting is such that \( V_{pd} \) is small, \( V_{pd} \) charges \( C \) through \( R \).

When this ramp voltage \( V_{C} \) reaches \( ZV_2 \), UJT fires.

Voltage \( V_{C} \) through the pulse transformer, is transmitted to the gate circuits of both SCRs. The forward biased \( T_1 \) is turned on. After this, \( V_{C} \) reduces to \( V_{pd} \) and then to zero at \( \theta = \theta_1 \). As \( V_{C} \) is more than \( V_{pd} \), during the charging of capacitor \( C \) through charging resistor \( R \), diode \( D \) is reverse biased and turned off. Thus \( V_{pd} \) does not effect in any way the discharge of \( C \) through UJT emitter and primary of pulse transformer. From 0 to \( T_1 \), \( T_1 \) is forward biased and is turned on. From \( T_1 \) to \( 2\pi \), \( T_2 \) is forward biased and is turned on.

In this manner, load is subjected to alternating voltage \( V_{pd} \) as shown in fig.

With the setting of wiper on \( R_2 \), pedestal voltage \( V_{pd} \) on \( C \) can be adjusted. With low pedestal voltage across \( C \), ramp charging of \( C \) to \( ZV_2 \) takes longer time, \( f_2 \) is firing angle delay is therefore more and output voltage is low.

With high pedestal on \( C \), voltage ramp charging of \( C \) through \( R \) reaches \( ZV_2 \) faster, firing angle delay is smaller, \( f_2 \) is output voltage is high. This shows that the output voltage is proportional to the pedestal voltage.

[Handwritten notes and equations]
Ratings

Thyristor ratings indicate voltage, current, power and temperature limits within which a thyristor can be used without damage or malfunction. Rating specifications serve as a link between the designer and the user of SCR systems.

For reliable operation of a thyristor, it should be ensured that the current and voltage ratings are not exceeded during its working. One of the major disadvantages of thyristors is that they have low thermal time constant. If a thyristor handles voltage, current and power greater than its specified rating, the junction temperature may rise above the safe limit and as a result the thyristor may get damaged. Therefore, when SCRs are selected, some safety margin must be kept in the form of choosing device ratings somewhat higher than their normal working values.

Anode Voltage Ratings

A thyristor is made up of four layers of three junctions. The anode voltage rating indicates the values of maximum voltages that a thyristor can withstand without a breakdown of the junction area with gate circuit open.

For an AC system, the supply voltage may not be a smooth sine wave. The voltage transients may occur regularly or at random as shown in fig. The different anode voltage ratings are:

1. \( V_{D_{w}} \) (Peak working forward blocking voltage): It specifies the maximum forward-blocking voltage that a thyristor can withstand during its working. Fig shows that \( V_{D_{w}} \) is the maximum value of the sine voltage wave.
Subscript letters indicate the dimension in mm. and kilo.

P = forward-blocking region with gate open, T = on state.
F = Forward, B = Blocking.
W = Working value, R = Repetitive value, S = Surge, M = Non-repetitive.
D = Maximum or peak value.

Fig: Anode voltage rating during the blocking state of a thyristor.

2) \( V_{\text{BRM}} \) (Peak repetitive forward-blocking voltage):

It refers to the peak transient voltage that a thyristor can withstand repeatedly or periodically in its forward-blocking mode. The rating is specified at a maximum allowable junction temp. with gate circuit open or with a specified biasing resistance between gate and cathode.

The voltage \( V_{\text{BRM}} \) is encountered when a thyristor is commutated or turned off. It may be recalled that during turn-off process, an abrupt change in reverse recovery current is accompanied by a spike voltage \( \frac{d}{dt} \); this is responsible for the appearance of \( V_{\text{BRM}} \) across the thyristor terminals.

3) Peak \( V_{\text{DSM}} \) (Peak surge, or non-repetitive forward-blocking voltage):

It refers to the peak value of the forward surge voltage that does not repeat. Its value is about 130% of \( V_{\text{BRM}} \), but \( V_{\text{DSM}} \) is less than \( V_{\text{BO}} \).
iv) \( V_{\text{RWM}} \) (Peak working reverse voltage):

It is the maximum reverse voltage that a thyristor can withstand repeatedly. Actually, it is equal to the peak negative value of a sine wave.

v) \( V_{\text{RRM}} \) (Peak repetitive reverse voltage):

It specifies the peak reverse transient voltage that may occur repeatedly in the reverse direction at the allowable maximum junction temp. The transient lasts for a fraction of the time of one cycle. The reason for the periodic appearance of \( V_{\text{RRM}} \) is the same as for \( V_{\text{RWM}} \).

vi) \( V_{\text{RSM}} \) (Peak surge (or non-repetitive) reverse voltage):

It represents the peak value of the reverse surge voltage that does not repeat. Its value is about 1.25\( V_{\text{RRM}} \). But \( V_{\text{RSM}} \) is less than \( V_{\text{RMR}} \).

vii) \( V_I \) (On-state voltage drop):

It is the voltage drop between anode & cathode with specified forward on-state current & junction temp. Its value is of the order of 1-1.5V.

viii) \( \frac{dV}{dt} \) (rate of rise of voltage)

The \( \frac{dV}{dt} \) rating of a thyristor indicates the maximum rate of rise of the anode voltage that will not trigger the device without any gate signal. If \( \frac{dV}{dt} \) is more than the specified maximum value, the thyristor may be switched on.
Current Ratings:

A thyristor is made up of a semiconductor material, and its thermal capacity is therefore quite small. Even for short overcurrent, the junction temperature may exceed the rated value and the device may be damaged.

1) Average On-state Current (I_{avg})

The forward voltage drop across conducting SCR is low, therefore power loss in a thyristor depends primarily on forward average on-state current \( I_{avg} \). For the purpose of illustrating the significance of average on-state current, consider a continuous dc current of flowing through the SCR, \( I_{dc} \).

\[ \text{Fig. Variation of Junction Temp.} \]

After application of this current at \( t=0 \), junction temp. begins to rise until finally it reaches its rated value \( T_j = 125^\circ C \). As the SCR has low thermal time constant, \( 125^\circ C \) is reached in a relatively short time.

2) RMS Current (\( I_{rms} \))

Heating of the resistive elements of a thyristor, such as metallic joints, leads, and interfaces, depends on the forward rms current \( I_{rms} \). The rms current rating is used as an upper limit for constant as well as pulsed anode current rating of the thyristor. Its value is equal to \( I_{dc} \).
iii) Surge Current Rating:

When a thyristor is working under its repetitive voltage and current rating, its permissible junction temp is never exceeded. However, a thyristor may be subjected to abnormal operating conditions due to fault or short circuits. In order to accommodate these unusual working conditions, surge current rating of thyristors is also specified.

A surge current rating indicates the maximum possible non-repetitive fault or short circuits should occur once in a while during the life span of a thyristor to prevent its degradation.

iv) \( I^2t \) Rating:

This rating is employed in the choice of a fuse or other protective equipment for thyristors. The rating in terms of amp²-sec specifies the energy that the device can absorb for a short time before the fault is cleared. It is usually specified for overloads lasting for less than or equal to one-half cycle of 50 or 60 Hz supply.

The \( I^2t \) rating is given by the relation

\[
\text{new value of one-cycle surge current} = \frac{I^2 t \text{ time for cycle}}{I^2 t \text{ for previous cycle}}
\]

For example, \( I^2t \) rating for 4A (min) SCR is 10 amp²-sec & for 35 A SCR is 160 amp²-sec.

In order that a fuse protects a thyristor reliably, the \( I^2t \) rating of fuse must be less than \( I^2t \) rating of the series-connected thyristors.

v) \( \frac{dI}{dt} \) Rating:

This rating of a thyristor indicates the maximum rate of rise current from anode to cathode, when a thyristor turns on, conduction starts at a place near the gate. This value is in terms of current strength in the whole area of junction.
If the $dV/dt$ is large as compared to the spreading velocity of carriers across the cathode junction, local hot spots will be formed near the gate connection as account of high current density. This causes the junction temperature above the safe limit and as a consequence, SCR may be damaged permanently.

**Other ratings:**

In addition to the voltage & current ratings of SCRs, there are some other ratings as under:

1. Latching and holding currents,
2. Turn-on & turn-off times,
3. Gate circuit voltage, current & power ratings

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Thyristor Protection

Reliable operation of a thyristor demands that its specified ratings are not exceeded. In practice, a thyristor may be subjected to overvoltages and overcurrents. During SCR turn-on, $di/dt$ may be prohibitively large. These may be false triggering of SCR by high value of $di/dt$. A spurious signal across gate-cathode terminals may lead to unwanted turn-on. A thyristor must be protected against all such abnormal conditions for satisfactory and reliable operation of SCR circuit.

1. $di/dt$ Protection

When a thyristor is forward biased and is turned on by a gate pulse, conduction of anode current begins in the immediate neighborhood of the gate-cathode junction, $J_g$. Thereafter, the current spreads across the whole area of junction. The thyristor design permits the spread of conduction to the whole area of junction as rapidly as possible. However, if the $di/dt$ is large as compared to the spread velocity of carriers, a local hot spot will be formed near the gate connection on account of high current density. The localised heating may destroy the thyristor. Therefore, the rate of rise of anode current at the time of turn-on must be kept below the specified limiting value. The value of $di/dt$ can be maintained below acceptable limit by using a small inductor, called $di/dt$ inductor, in series with the anode circuit.

Typical $di/dt$ limits value of SCR are $20-500 \ A/\mu s$. 
With a forward voltage across the anode-cathode junction of a thyristor, the two outer junctions are forward biased but inner junction is reverse biased (J2), has the characteristics of a capacitor due to charges existing across the junction. If the entire anode is cathode forward voltage appears across J2 junction and the charge is denoted by \( Q \), then a charging current \( i \) given by:

\[
i = \frac{dQ}{dt} = \frac{d}{dt} (C_j \cdot V_a) = C_j \frac{dV_a}{dt} + V_a \frac{dC_j}{dt}
\]

As \( C_j \), the capacitance of junction J2 is almost constant, the current is given by:

\[
i = C_j \frac{dV_a}{dt}
\]

If the rate of rise of forward voltage \( \frac{dV_a}{dt} \) is high, the charging current \( i \) will more. This charging current plays the role of gate current and turns on the SCR even when gate signal is zero. Such phenomena of turning on a thyristor called \( \frac{dV_a}{dt} \) turn-on, operation of thyristor must be avoided as it leads to false operation of thyristor circuit.

For controllable operation of thyristor, the rate of rise forward anode to cathode voltage \( \frac{dV_a}{dt} \) must kept below the specified limit. Typical values of \( \frac{dV_a}{dt} \) are \( 20-500 \text{ V/s} \) per False turn-on of a thyristor by large \( \frac{dV_a}{dt} \) can be prevented by using a snubber circuit in parallel with the device.
Design of Snubber Circuit

A snubber circuit consists of a device combination of resistance $R_s$ and capacitance $C_s$ in parallel with the transistor as shown in Fig. A capacitor in parallel with the device is sufficient to prevent unwanted $dV/dt$ triggering of the SCR. When switch $S$ is closed, a sudden voltage appears across the circuit. Capacitor $C_s$ across behaves like a short circuit, therefore voltage across $C_s$ is zero. When the passage of time voltage across $C_s$ builds up at a slow rate such that $dV/dt$ across $C_s$ is therefore across SCR is less than specified maximum $dV/dt$ rating of the device.

Here the question arises that if $C_s$ is enough to prevent accidental turn-on of the device by $dV/dt$?

Before SCR is fired by gate pulse, $C_s$ charge to full voltage $V_s$. When SCR is turned on, capacitor discharges through SCR and sends a current equal to $V_s/(resistance\ of\ local\ path\ formed\ by\ cs\ &\ scr)$. As this resistance is quite low, the turn-on $dI/dt$ will tend to be excessive and as a result, SCR may be destroyed. In order to limit the magnitude of discharge current, a resistance $R_s$ is inserted in series with $C_s$ as shown in Fig. Now when SCR is turned on, initial discharge current $V_s/R_s$ is relatively small and turn-on $dI/dt$ in reduced.
Gate Turn-Off Thyristors (GTO thyristor)

Thyristors are nearly the ideal switch for use in power electronic applications. They can block high voltages (several thousand volts) in the off state and conduct large current (several thousand amperes) in the on state with only a small on-state voltage drop (a few volts). Most useful of all is their capability of being switched on and off by means of a control signal applied at the gate of the thyristor.

However, the thyristor has a serious deficiency that prevents its use in switch-mode applications: the inability to turn-off the device by application of a control signal at the thyristor gate. The inclusion of a turn-off capability in a thyristor requires device modifications and some compromises in the operational capabilities of the device. We would see the structure and operation of thyristors that have a gate turn-off capability, the so-called GTO thyristor, usually abbreviated as GTO, and the performance compromises required to achieve turn-off capability. A GTO requires a positive current pulse at the gate for turn-on and a negative current pulse for turn-off.

Some of the structural differences vis the thyristor are as follows:

1. The P layer is thinner than in thyristor,
2. Cathode periphery is maximized by building cathode as small islands,
3. The gate to cathode distance is minimized,
4. The P layer is shorted to the anode, called the anode short structure, is used to speed-up the turn-off of the GTO.

Fig 1 shows the structure and symbol of a GTO.

The anode short is implemented by diffusing N⁺ (n⁺) beads directly below the anode islands. The shorting speeds up the turn-off process. It effectively short the junction, which, if you recall the thyristor, was responsible for withstanding almost reverse blocking voltage, but in GTO reduced the reverse blocking capability (approximately 20 to 30 volts).
Fig. Structure of GTO

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Fig. Symbols of GTO

Since the GTO is primarily intended for dc applications, the reduced reverse blocking capability is not important.

The island structure of GTOs makes it necessary to apply higher positive gate current pulses than a thyristor for turn-on.

The turn-off gate current diverts the hole from p-box region to the gate terminal.

In the equivalent circuit both Q1 & Q2 are saturated in thyristors on state. However, if

\[ I_{c1} = I_{c2} \]

the base current to Q2 could briefly be made less than the value needed to maintain saturation.

Fig. Two transistor analogy (\( I_{B2} < I_{c2}/\beta_2 \)),

Q2 (GTO equivalent circuit) then Q2 would go active and the thyristor would begin to turn-off because of the regeneration action present in the circuit when one or both of the transistors are active.
Using the equivalent circuit we can write $I_{B2}$ in terms of the thyristor terminal current as:

$$I_{B2} = \alpha_1 I_A - I_0'$$  \(\text{(1)}\)

where $I_0'$ is the negative of the normal gate current.

From the equivalent circuit it is clear that a negative gate current $I_0'$ is the only way that $Q_2$ can be brought out of saturation. The collector current $I_{C2}$ can be expressed as:

$$I_{C2} = I_e - I_{B1}$$

$$I_{B1} = I_{C2} - I_{E1} - \alpha_1 I_{E1} = I_A - \alpha_1 I_A$$

$$I_{C2} = \frac{1}{1 - \alpha_1} I_A$$  \(\text{(2)}\)

Setting up the inequality $I_{B2} < I_{C2} / \beta_2$ with $\beta_2 = \frac{\alpha_2}{1 - \alpha_2}$

Then using $\alpha_2 < \beta_2$ and $\beta_2 < I_{C2}$ yield:

$$I_{B2} \beta_2 < I_{C2}$$

$$(\alpha_2 I_A - I_0') \beta_2 < (1 - \alpha_1) I_A$$

$$(\alpha_1 I_A - I_0') \frac{\alpha_2}{1 - \alpha_2} < (1 - \alpha_1) I_A$$

$$\alpha_1 \alpha_2 I_A - I_0' \alpha_2 < (1 - \alpha_1) (1 - \alpha_2) I_A$$

$$\alpha_1 \alpha_2 I_A - I_0' \alpha_2 < (1 - \alpha_2 - \alpha_1 + \alpha_1 \alpha_2) I_A$$

$$\alpha_1 \alpha_2 I_A - I_0' \alpha_2 < (1 - \alpha_1 - \alpha_2) I_A + \alpha_1 \alpha_2 I_A$$

$$I_0' < \frac{\alpha_2}{(\alpha_1 + \alpha_2 - 1)}$$

$$I_0' < \frac{I_A}{\alpha_2 (\alpha_1 + \alpha_2 - 1)}$$

$$I_0' < \frac{I_A}{\beta_{off}}$$

The parameter $\beta_{off}$ is the turn-off gain and is given by:

$$\beta_{off} = \frac{\alpha_2}{\alpha_1 + \alpha_2 - 1}$$
A large value of $I_f$ is desirable. Typical value is in the range 2 to 10. The turn-off gain is small, hence large negative gate current pulses are needed for turning off, but a large amount of negative current crowding makes the maximum current a GTO can turn off is limited. Hence, large value of negative gate current can be avoided.

For that some structural modification are required.

1) $\alpha_2$ should be near unity & $\alpha_1$ should be small.
2) Making $\alpha_2$ near unity involves the use of a narrow $P_2$ layer for the npn transistor $Q_2$ & use of heavy doping in the $n_2$ cathode layer (emitter of $Q_2$)
3) To make $\alpha_1$ small, the wide $n_1$ region above $Q_1$ is also needed for large blocking voltage.
4) Short lifetime in $n_1$ region to remove excess minority carrier rapidly so $Q_1$ can turn off.

The i-v characteristics of a GTO are similar to those of the thyristor.

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Insulated Gate Bipolar Transistor (IGBT)

BJT & MOSFET's have characteristics that complement each other in some respects.

<table>
<thead>
<tr>
<th>BJT</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Lower conduction losses</td>
<td>1. Turn-on &amp; off much faster</td>
</tr>
<tr>
<td></td>
<td>in on state, especially in device with larger blocking voltage.</td>
</tr>
<tr>
<td>2. Have longer switching time, especially at turn-off</td>
<td>2. Faster on-state conduction losses are larger, especially in devices rated for higher blocking voltage.</td>
</tr>
</tbody>
</table>

These observations have led to attempts to combine BJT's & MOSFET's monolithically on the same silicon wafer to achieve a circuit or even perhaps a new device that combines the best qualities of both types of devices. These attempts have led to the development of the IGBT, which is becoming the device of choice in most new applications.

Basic Structure:

![Diagram of IGBT structure]

The structure is quite similar to that of the vertical diffused MOSFET. The principal difference is the presence of the p+ layer that forms the drain of the IGBT. This layer forms a p-n junction (called J3), which injects minority carriers that would be repelled to the drain region of the MOSFET. The gate & source of the IGBT are laid out in an
In contrast, the geometry similar to that used for the vertical MOSFET.

The doping levels used in each of the IGBT layers are similar to those used in the comparable layers of the MOSFET structure except for the body region.

The IGBT structure has a parasitic thyristor. Turn-on of this thyristor is undesirable in several structural details of a practical IGBT geometry, principally in the p-type body region that forms junctions J2 and J3 are different from the simple geometry to minimize the possible activation of this thyristor.

![Fig. n-channel IGBT Circuit Symbol]

Fig. shows the circuit symbol for n-channel IGBT. Directions of the arrowheads would be reversed in a p-channel IGBT. This symbol is essentially the same as that used for an n-channel MOSFET, but with the addition of an arrowhead in the drain lead pointing into the body of the device, indicating the injecting contact.

There is some disagreement in the engineering community over the proper symbol to use with the IGBT. Some prefer to consider the IGBT as basically a BJT with a MOSFET gate input & thus use the modified BJT symbol for the IGBT.
Fig. 6: Output characteristics

The i-v characteristics of n-channel IGBT are shown in Fig. 6. In the forward direction, they appear qualitatively similar to those of a logic-level BJT except that controlling parameter in an input voltage, the 
gate-source voltage, rather than an input current.

The junction J2 blocks any forward voltages when 
the IGBT is off. The reverse-blocking voltage indicated 
on the i-v characteristic can be made as large as the 
forward blocking voltage if the device fabricated without 
the n+ buffer layer. Such a reverse-blocking capability 
is useful in some applications. The junction J1 is 
the reverse-blocking junction. However, n+ buffer layer 
used in device construction; the breakdown voltage 
of this junction is lowered significantly, to a few tens 
of volts, because of the heavy doping now present on 
both sides of this junction. The IGBT no longer 
has reverse-blocking capability.

The transfer curve I_d-Vgs shown in Fig. 6 is 
identical to that of the power MOSFET. The curve is 
reasonably linear over most of the drain current range 
becoming nonlinear only a low drain current where the 
gate-source voltage is approaching the threshold. If Vgs 
is less than the threshold voltage Vgs(th), then the 
IGBT is in the off state. The maximum voltage that 
should be applied to the gate-source terminals is usually 
limited by the maximum drain current that should be 
permitted to flow in the IGBT.
Field-Controlled Thyristor (FCT)

Fig 6 Basic structure

If the drain of a power JFET structure is modified into an injecting contact by making it into a pn junction, then a new device is produced. This new device, which is variously termed a field-controlled thyristor (FCT), a field-controlled diode and in Japan, a bipolar static induction thyristor (BSITy), has basic structure shown in Fig 6. Normally the drain of an n-channel JFET is converted into a pn junction & it becomes the anode of the device.

The source of the JFET portion of the new structure is now termed the cathode. The circuit symbol for the FCT is shown in Fig 6 & is essentially a diode symbol with a gate terminal added. The arrow on the gate terminal indicates the direction of forward bias current flowing into the gate-source pn junction.

Fig 6-1 Characteristics of a FCT

The i-v characteristic of a normally-on FCT is shown in Fig. In the forward bias portion of the characteristics, the FCT appears similar to power JFET. The direction difference in the forward-bias operation...
A two devices is quantitative, with the FET being able to conduct for larger currents than JFET for the same on-state voltage. The FET also blocks in the reverse direction because of the addition of the pin junction at the anode. This reverse blocking is independent of the voltage applied to the gate-source junction.
The MOS-controlled thyristor (MCT) is a new device that has recently become commercially available. It is basically a thyristor with two MOSFETs built into the gate structure with one of the two MOSFETs, the ON-FET responsible for turning the MCT on and other MOSFET, the OFF-FET responsible for turning the device off. There are two types of MCTs—(a) P-MCT, (b) N-MCT. Both combine the low on-state losses and large current capability of thyristors with the advantages of MOSFET-controlled turn-on & turn-off and relatively fast switching speeds.

Cross-sectional view of a single cell of a P-MCT is shown in Fig. 1. A complete P-MCT is composed of many thousands of these cells fabricated integrally on the same silicon wafer and all the cells are connected electrically in parallel. The thyristor portion of the device has the same structure as a
conventional Thyristor. The P-region nearest to the cathode, the base region of the npn transistor in
the two-BJT model of the thyristor section in fig 0, is the lightly doped region that must contain the
depletion region of the blocking junction J₂ when the device is off. The ON-FET is a p-channel
MOSFET & OFF-FET is an n-channel MOSFET.
These MOSFETs are located around the anode
of MCT as shown in fig 0, and thus the MOSFETs
share the same side or surface of the silicon
wafer as the anode.

   Every cell contains an OFF-FET, but most
cells do not have an ON-FET. Typically about
1 out of 20 cells contains an ON-FET. Because
of the close packing of the cells, if one cell
turns on, it will cause adjacent cell to turn-on
because some of the excess carriers in the cell
with the ON-FET will able to diffuse to the
adjacent cell & thus provide them with the
excess carriers needed for turn-on.

   An equivalent circuit for P-MCT is shown
in fig 0 & it includes not only the two-BJT
model of the thyristor portion of the device but
also the ON-FET & OFF-FET. The circuit symbol
for P-MCT is shown in fig 0.

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A cross-sectional view of a single cell of N-MCT is shown in Fig 1. Like the P-MCT, a complete N-MCT is composed of many thousand of cells fabricated integrally on the same silicon wafer & all the cells are connected electrically in parallel. The Thyristor portion of the device has the same pnpn structure as a conventional Thyristor. The lightly doped region must contain the depletion layer of the blocking junction. It is placed in the n-type region nearest to the anode. This p-type region also functions as the base of the pnp transistor in the two BJT model of the Thyristor.

The ON-FET is a n-channel MOSFET & the OFF-FET is an n-channel MOSFET. The MOSFET are
located around the cathode, as shown in fig. 1, and share same side of silicon wafer as the cathode.

Every cell contains an OFF-FET, but only about 1 in 20 cells has an ON-FET.

An equivalent circuit for the N-MCT is shown in fig. 2, and it includes not only the two-JET model of the thyristor portion but also the ON-FET & OFF-FET.

The circuit symbol for the N-MCT is shown in fig. 8.3.

The i-v characteristics of both types of MCTs is essentially the same as for a GTO.

P.J. Shah
Electrical Isolated Driver Circuit for IGBT & MOSFET

The basic ways to provide electrical isolation are either by optocouplers, fiber optics, or by transformers. 

![Diagram of an isolated drive circuit](image)

Input to remainder of isolated drive circuit

Power switch reference node (emitter or source)

Fig. Schematic of an optocoupler used to couple signals to a floating (electrically isolated) drive circuit from a control circuit referenced with respect to the control logic ground.

The optocoupler shown in Fig. (above) consists of a light-emitting diode, output transistor and a built-in Schmitt trigger. A positive signal from the control logic causes the LED to emit light that is focused on the optically sensitive base region of a photo transistor. The light falling on the base region generates a significant number of electron-hole pairs in the base region that causes the photo transistor to turn-on. The resulting drop in voltage at the photo transistor collector causes the Schmitt trigger to change state. The output of the Schmitt trigger in the optocoupler output and can be used as the control input to the isolated drive circuit.

The capacitance between the LED and the base of the receiving transistor within the optocoupler should be as small as possible to avoid retriggering at both turn-on & turn-off of the power transistor due to the jump in the potential between the power transistor emitter reference point and the


ground of the control electronics. To reduce this problem, optocouplers with electrical shields between the LED and the receiver transistor should be used.

As an alternative, fiber optic cables can be used to completely eliminate this retriggering problem and to provide very high electrical isolation and creepage distance.

When using fiber optic cables, the LED is kept on the printed circuit board of the control electronics, and the optical fiber transmits the signal to the receiver transistor, which is put on the drive circuit PCB.

Instead of using optocouplers or fiber optic cables, the control signal can be coupled to the electrically isolated drive circuit by means of a transformer, as shown in Fig. 1 below.

Fig. 1 Electrically isolated drive circuit.

If switching frequency is high (kHz or more) and the duty ratio D varies only slightly around one, a baseband control signal of appropriate magnitude can be applied directly to the primary of a relatively small and lightweight iron-core transformer. This isolated output can be used to either directly drive the power switch or used as the input to an isolated driver circuit. As the switching frequency is decreased below the tens of kHz range, a baseband control signal directly applied to the transformer primary becomes
Optocoupler - isolated drive circuits

Optocoupler - isolated drive circuits can also be used with power MOSFETs & IGBTs. The circuit shown in Fig. (above) uses a high common-mode noise immunity optocoupler and high-speed driver with a 3A output capability. The drive circuit uses a single-ended floating 15V supply and provides a ±15V output voltage for high noise immunity and fast switching to drive the gate of a power MOSFET or IGBT. The integrated high-speed driver circuit connects the gate of the power device to the ±15V bus bar while it simultaneously connects the source to the negative side of the bias supply in order to turn-on the power device. To turn-off the power device, the power circuit connects the gate to the negative side of the single-ended supply while it connects the source to the +15V bus bar.

In this way electrical isolation needed between the logic-level control signals & the drive circuits.